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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,260	04/13/2004	Katsumi Iwata	10-9602D	6495

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EXAMINER

COLEMAN, ERIC

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/824,260	Applicant(s) IWATA, KATSUMI	
	Examiner Eric Coleman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6 and 7 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 6 and 7 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Specification

The applicant is reminded that the serial numbers of the applications and patent numbers of issued patents to which the applicant claims priority under 35 U.S.C. 120 in the instant application should be contained in the first sentence of the specification. Correction is required.

Claim Rejections - 35 USC § 103

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smayling (US patent No. 5,642,295) in view of Japanese patent 3-45299 (hereafter referred to as '45299 submitted by applicant) or Yukio (Japanese patent publication number 07-261997) (abstract submitted by applicant).

1. Smayling taught the invention substantially as claimed including a data processor formed on a semiconductor substrate (microcontroller chip 22, e.g. see fig. 3, e.g., see col. 6, lines 3-7 and col. 6, lines 44-54) comprising:

a) Electrically erasable or programmable non-volatile memory (EEPROM 52 e.g., see fig. 3);

b) Central Processing Unit (46) capable of accessing the non-volatile program memory (e.g., see figs. 3, and 3a and col. 6, lines 44-54)[the EEPROM is taught as storing a program that is run by the CPU, this requires the access of the program by the CPU from the program memory]; and

c) Control circuit (e.g., see col. 6 lines 44-54)[CPU includes a controller].

2. Smayling did not expressly detail (claim 6) the operation control circuit terminating a process for erasing or programming of data in an EEPROM in response to an interrupt during erasing or programming.

3. The ' 45299 reference however taught (claim 6) a system that comprises a signal that controls whether or not the process of erasing of the EEPROM is to be terminated or not during an interrupt request. Therefore it with this control it would have been obvious to one of ordinary skill that when the control was set for terminating the erasing then the erasing would have been terminated during an interrupt (e.g., see fig. 2c, and page 6, line 7- lines 12).

4. Yukio taught (claim 6) a flash memory and flash ROM write deletion management control program that manages write or deletion to the flash ROM. Yukio also taught while the write or the like is being performed, only the interruption request of a high priority degree is permitted. Thus write or deletion is performed to the flash ROM storing the management program (see abstract).

5. As per claim 7, Smayling did not expressly detail the operation control circuit excluding an interrupt request or exception processing request to the CPU during erasing or programming. The ' 45299 reference however taught excluding an interrupt request to the CPU during erasing or programming of data in EEPROM in accordance with the request for erasing or programming the data in the EEPROM (e.g., see fig 2b and page 4, line 11-page 5, line 21).

6. Also (claim 7) Yukio taught a flash memory and flash ROM write deletion management control program that manages write or deletion to the flash ROM. Yukio

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also taught while the write or the like is being performed, only the interruption request of a high priority degree was permitted.

7. It would have been obvious to combine the teachings of Smayling and the '45299 reference. Both references were directed toward the problems of using an Electrically erasable programmable memory for storage of data in a DP system. The incorporation of the '45299 teachings of detecting a condition for determining whether to interrupt an erasing or writing process during a power failure into the Smayling system would have enabled the combined system to ensure that valuable program instructions and/or data would not be lost during an interruption of programming or erasing of the EEPROM.

8. It would have been obvious to combine the teachings of Smayling and the Yukio reference. Both references were directed toward the problems of using an Electrically erasable programmable memory for storage of data in a DP system. The incorporation of the Yukio teachings of using a determining whether to interrupt an erasing or writing process during interrupts of different priorities into the Smayling system would have enabled the combined system to ensure that valuable program instructions and/or data would not be lost during an interruption of programming or erasing of the EEPROM.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Zimmermann (patent No. 5,712,969) disclosed a DP system for reprogramming erasable, non-volatile memory (e.g., see abstract).

Durante (patent No. 5,765,184) disclosed a system for programming an array controller in a flash memory device.


Shibata (patent No. 5,590,303) disclosed a memory designation control with mode for selecting whether to rewrite a flash memory and inhibition signal inhibiting writing the flash EEPROM (e.g., see col. 5, lines 29-63 and fig. 1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC


ERIC COLEMAN
PRIMARY EXAMINER